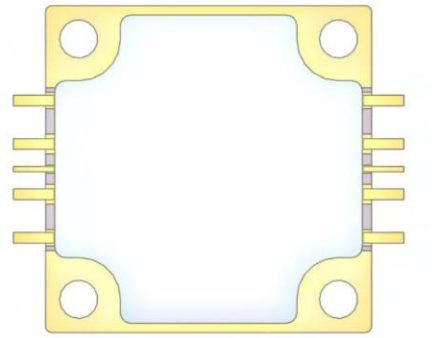
GaN MMIC
Power Amplifier
6-18GHz

Features

- Frequency: 6-18GHz
- Power Gain: 20dB
- Psat: 44.7dBm typ.
- PAE: 32%
- 50Ohm Input/Output
- Size: 15.24*15.24*3.8mm



Product Description

- RW6016P is a power amplifier based on GaN technology, the frequency range covers 6-18GHz, the power gain is 19.7dB, saturated output power of 44.7dBm. RW6016P use +28V power supply.

Electrical Specifications

TA = +25ºC, VD = +28V, VG=-1.8V, Pin=24dBm, CW mode, 50Ω system

Parameter	Symbol	Min.	Typ.	Max.	Units
Frequency	Freq		6-18		GHz
Saturated Output Power	Psat		44.7		dBm
Power Gain	Gp		20		dB
Power-added Efficiency	PAE		32		%
Quiescent Current	Idq		1.74		A

Thermal and Reliability Information

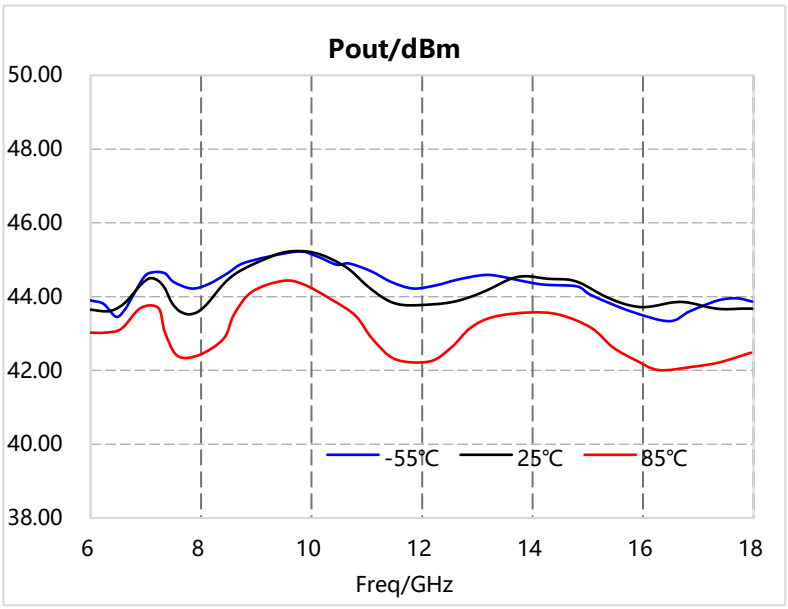
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})	Temp=85℃, VD=+28V, VG=-1.8V, Pin=24dBm, CW	1.3	℃/W
Channel Temperature, T_{CH}		156	℃

Absolute Maximum Ratings

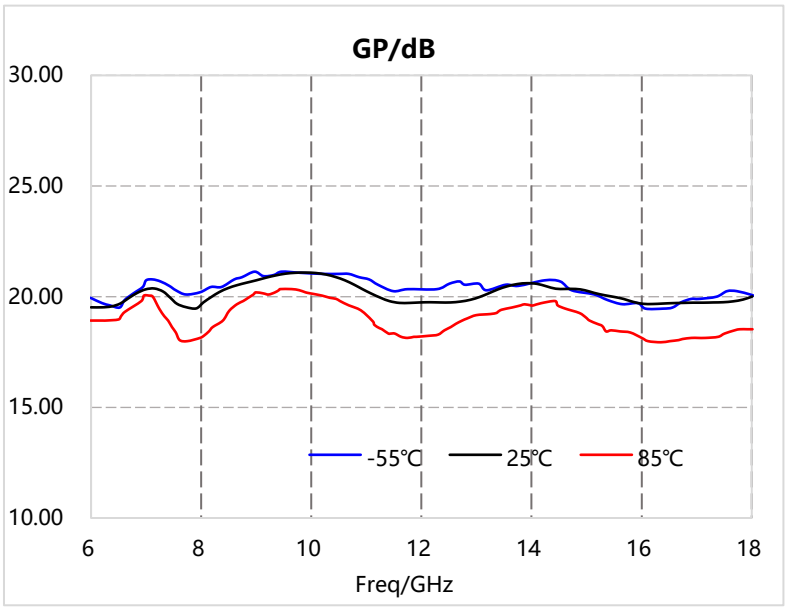
Maximum Drain voltage	+32V
Maximum Gate voltage	-5V
Maximum Input Power	+30dBm
Maximum Junction Temperature	+225℃
Sintering Temperature(30s, N2 protection)	+300 ± 10 °C
Operating Temperature	-55 ~ + 85°C
Storage Temperature	-65 ~ + 150°C
Exceeding any of the above maximum limits may cause permanent damage.	

Test Curve （Vd=+28V, Vg=-1.8V， IDQ=1.74A, Pin=24dBm, CW）

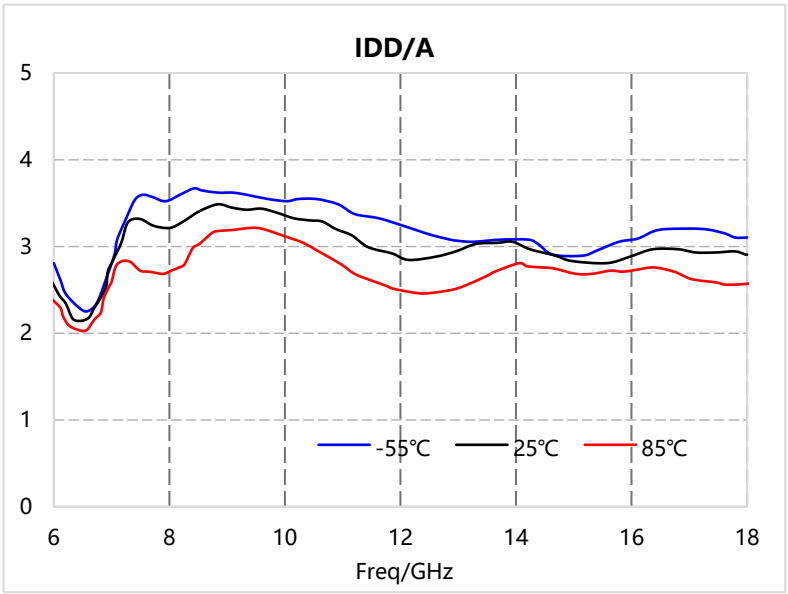
Psat vs. Frequency vs. Temperature



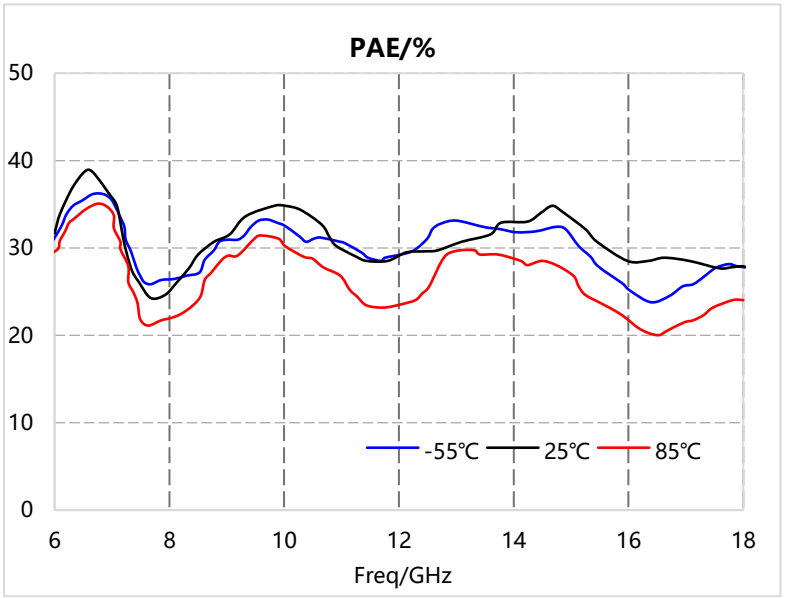
Power Gain vs. Frequency vs. Temperature



IDD vs. Frequency vs. Temperature

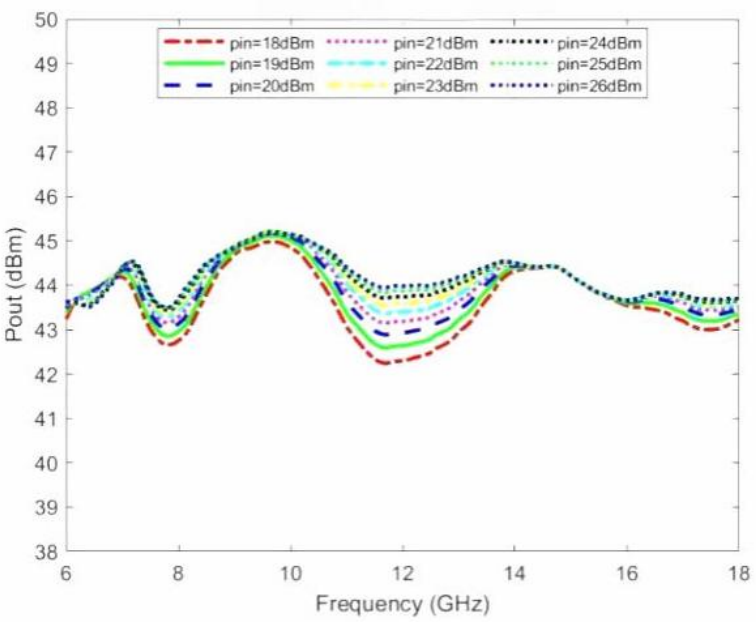


PAE vs. Frequency vs. Temperature

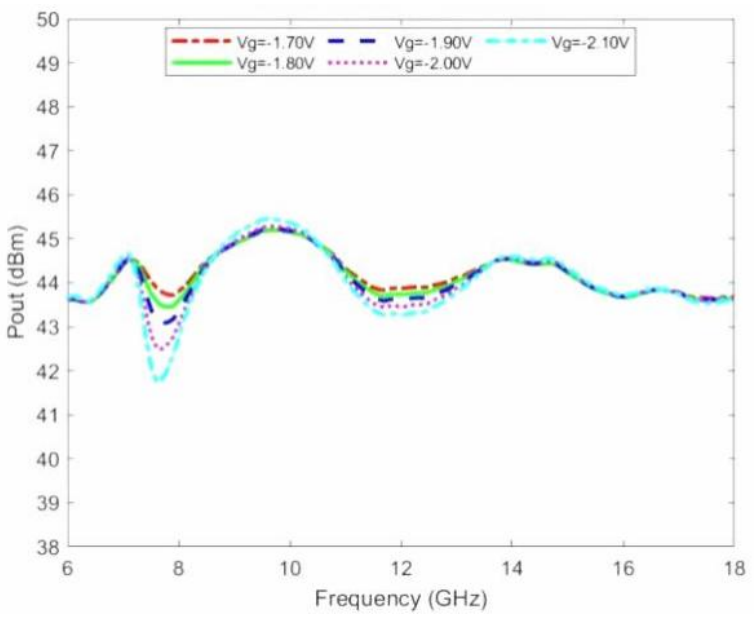


Test Curve （ TA = +25℃, Vd=+28V, Vg=-1.8V， IDQ=1.74A, CW）

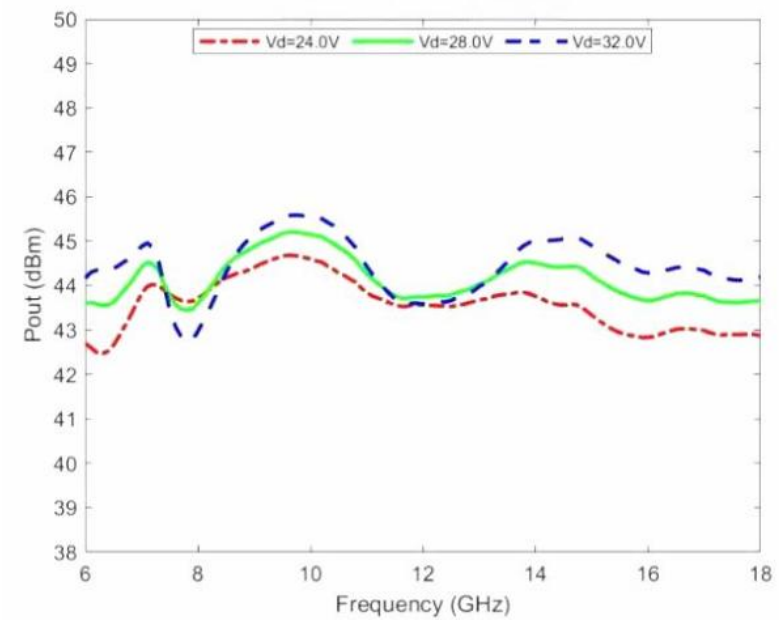
Pout vs. Frequency vs. Pin



Pout vs. Frequency vs. VG@Pin=24dBm

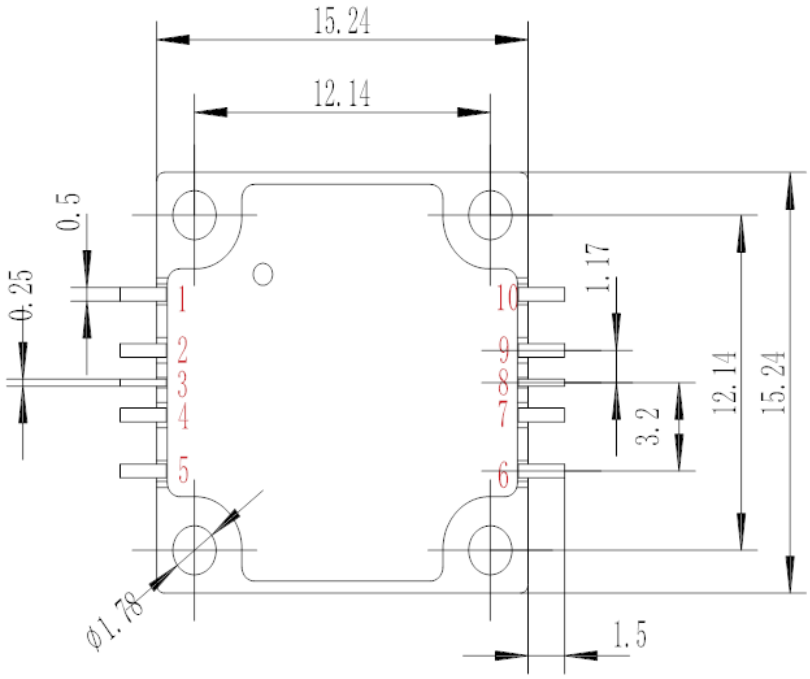


Pout vs. Frequency vs. VD@Pin=24dBm

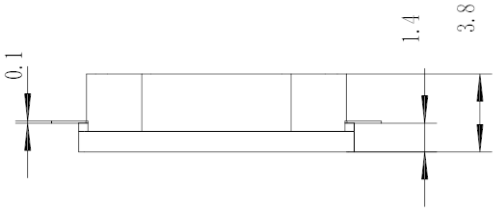


Outline Drawing

All Dimensions in mm



Top View



Side View

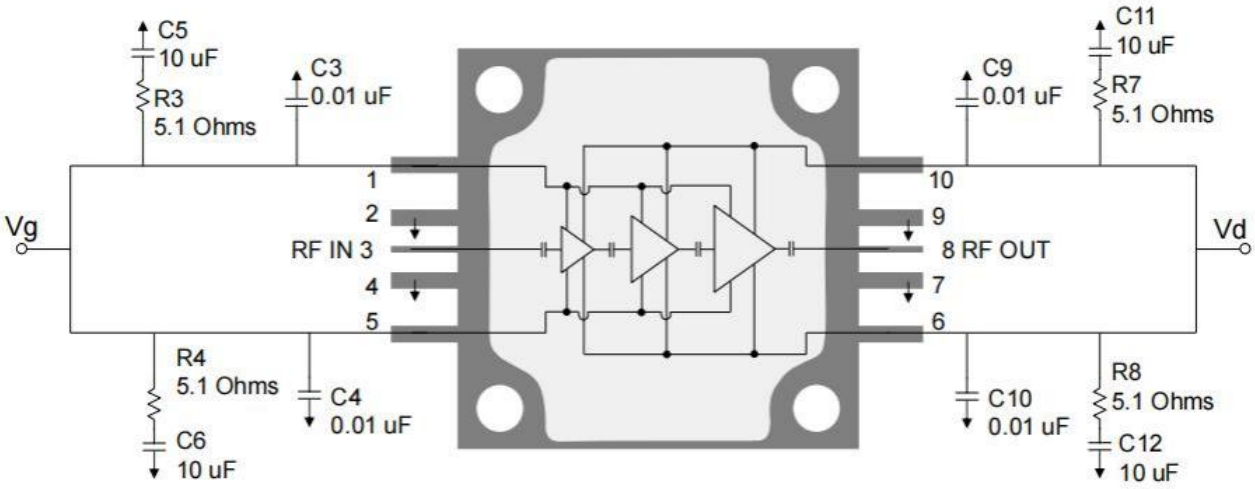
Materials:

Base: Copper
Lid: Ceramic
All metalized features are gold plated
Part is epoxy sealed

Pad Description

Pad No.#	Symbol	Function
3	RF IN	RF input pad, connected to 50Ω system, with DC blocking capacitor inside the chip
8	RF OUT	RF output pad, connected to 50Ω system, with DC blocking capacitor inside the chip
1	VG1	Gate Bias Voltage1, bias network is required.
5	VG2	Gate Bias Voltage2, bias network is required.
10	VD1	Drain Bias Voltage1, bias network is required.
6	VD2	Drain Bias Voltage2, bias network is required.
2,4,7,9	GND	RF Reference Ground

Assembly Drawing



1. Vg1 and Vg2 can be connected together (the same as Vd1 and Vd2).
2. Each gate (Vg1, Vg2) and each drain (Vd1, Vd2) must be biased

Assembly Notes

1.Carefully clean the PC board, base plate, and package leads with alcohol. Allow it to dry fully.

2.To improve the thermal and RF performance, recommends attaching a heat sink to the bottomof the package and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch(maximum thickness) Indium shim between the heat sink and the package.

3.The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the RW6016P. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. The package lead temperature should not exceed 260 deg C. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.

4.The packaged part should not be subjected to conventional SMT automated solder reflow processes.

5.Use screws to attach the component to the heat sink. A suggested final torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value.