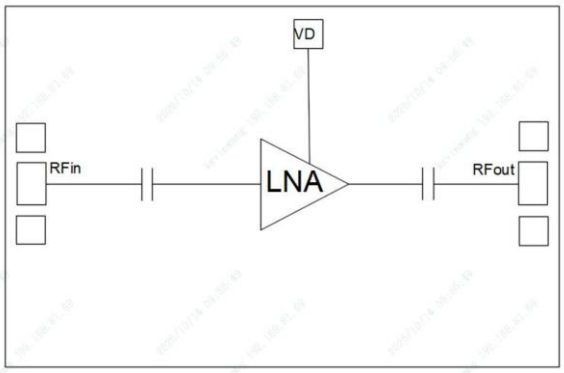
GaAs pHEMT MMIC
Low Noise Amplifier
1-4GHz

Features

- Single Biasing Voltage (Self Biased)
- Noise Figure: 0.33dB
- Gain: 28dB
- P1dB: 13dBm
- Biasing: +5V @ 32.1mA
- Impedance: 50Ω
- Die Size: 1.6 x 1.3 x 0.1 mm

Functional Block Diagram



Electrical Specifications

TA = +25ºC, VD = +5V, Idq = 32.1mA, Pin=-30dBm, 50Ω system, CW

Parameters	Min.	Typ.	Max.	Units
Frequency		1 - 4		GHz
Gain	27.8	28		dB
Gain Flatness		±0.15		dB
Noise Figure		0.33	0.4	dB
Input Return Loss		9		dB
Output Return Loss		15		dB
Output 1dB Compression (OP1dB)		13		dBm
Input 1dB Compression (IP1dB)		-14		dBm

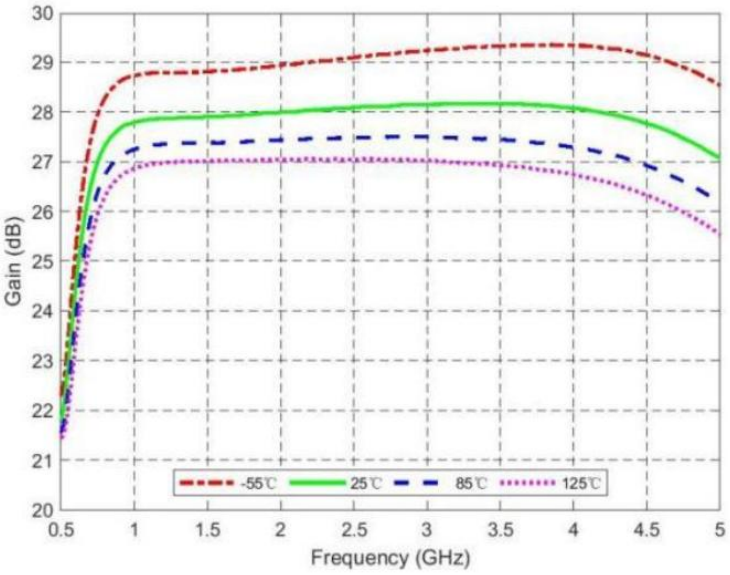
DC Characteristics

Parameters	Min.	Typ.	Max.	Units
Drain Voltage VD		5		V
Operating Current IDD@-55℃		35.6		mA
Operating Current IDD@+25℃		32.1		mA
Operating Current IDD@+85℃		30.5		mA
Operating Current IDD@+125℃		29.8		mA

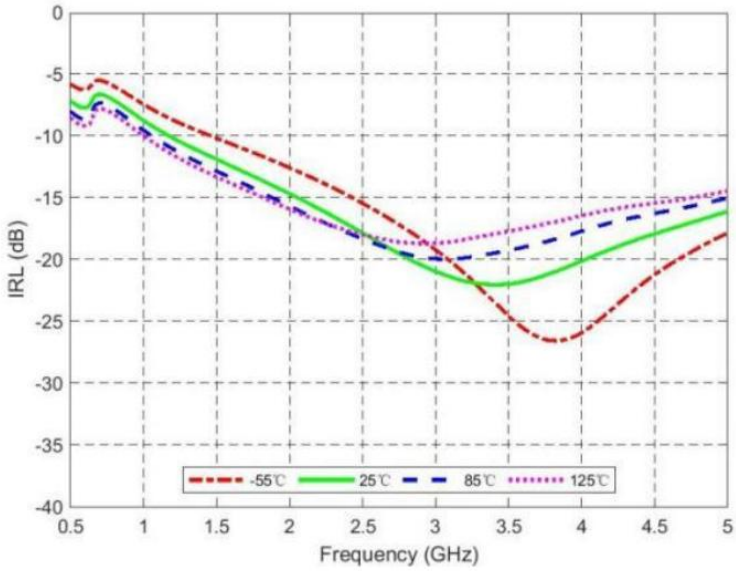
Test Curve

VD = +5V, Idq = 32.1mA, Pin=-30dBm, 50Ω system, CW

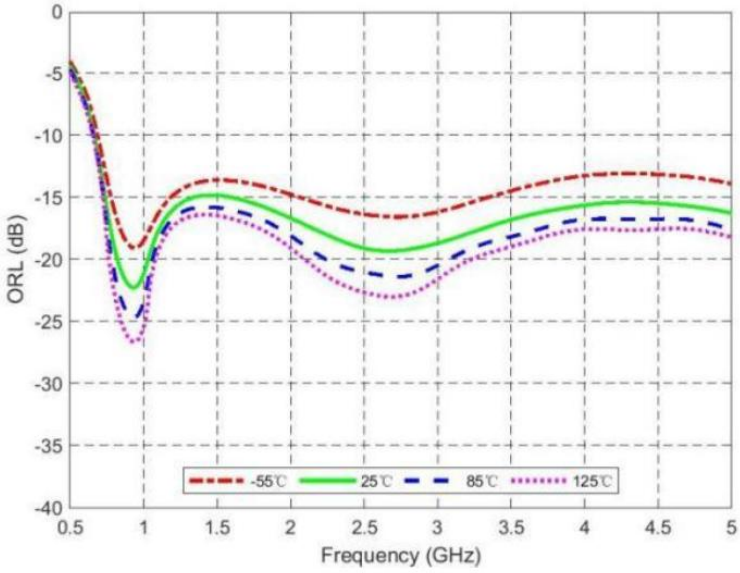
Gain vs. Frequency vs. Temperature



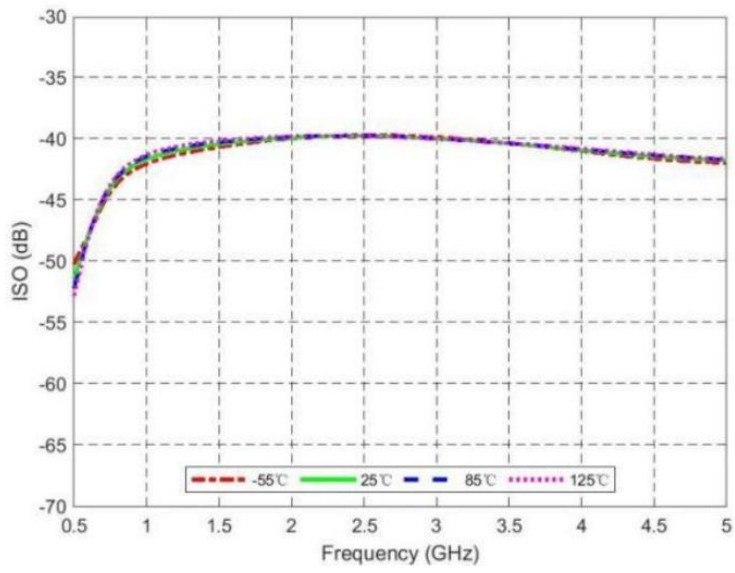
Input RL vs. Frequency vs. Temperature



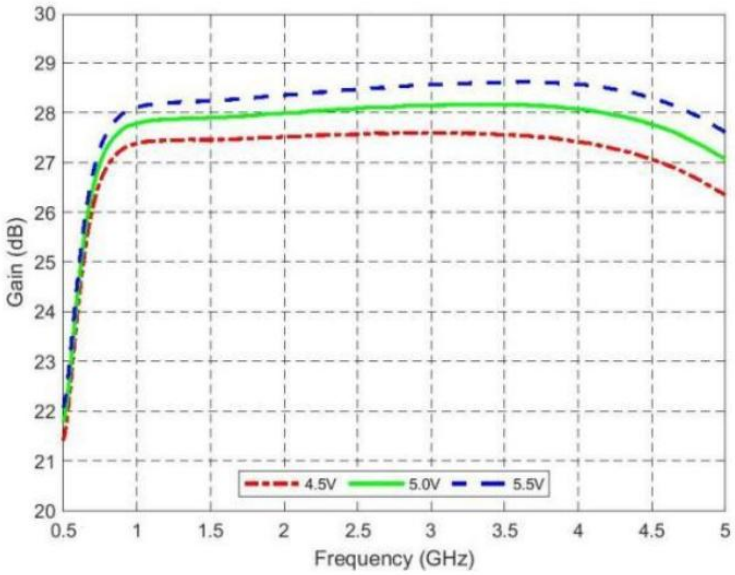
Output RL vs. Frequency vs. Temperature



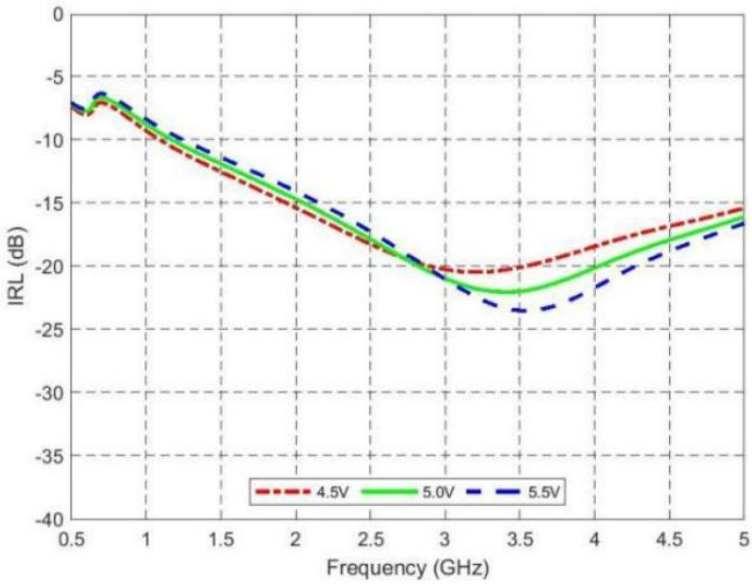
Isolation vs. Frequency vs. Temperature



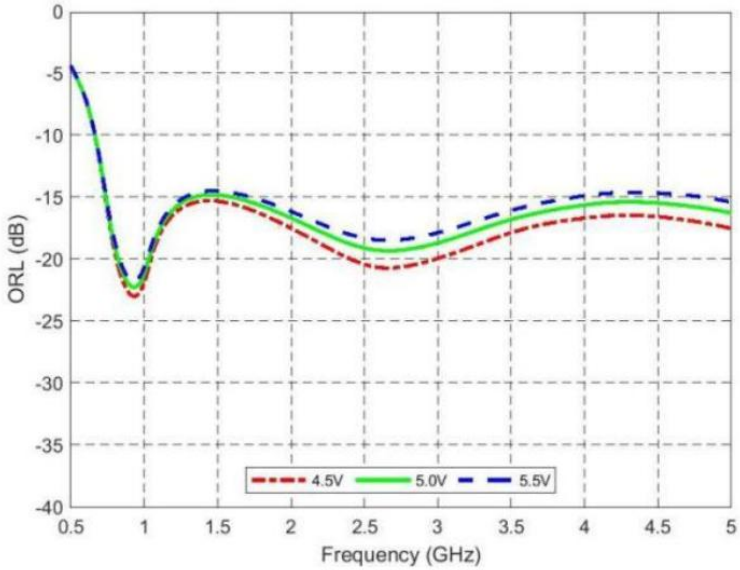
Gain vs. Frequency vs. VD



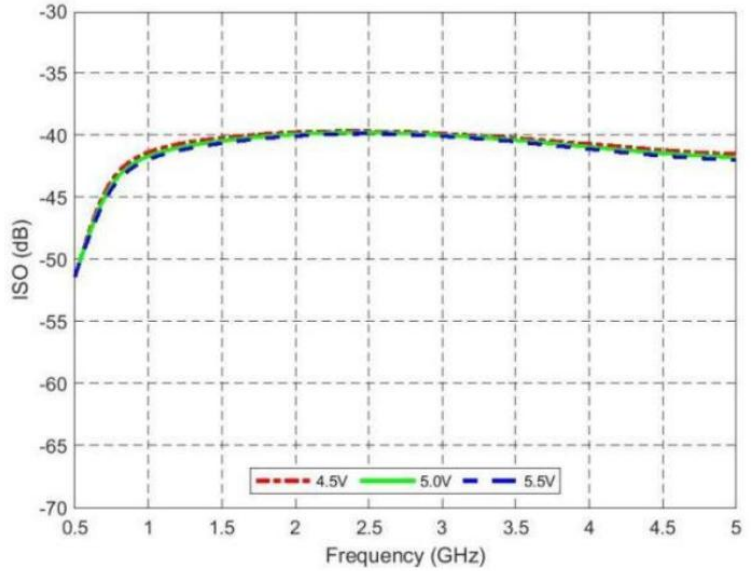
Input RL vs. Frequency vs. VD



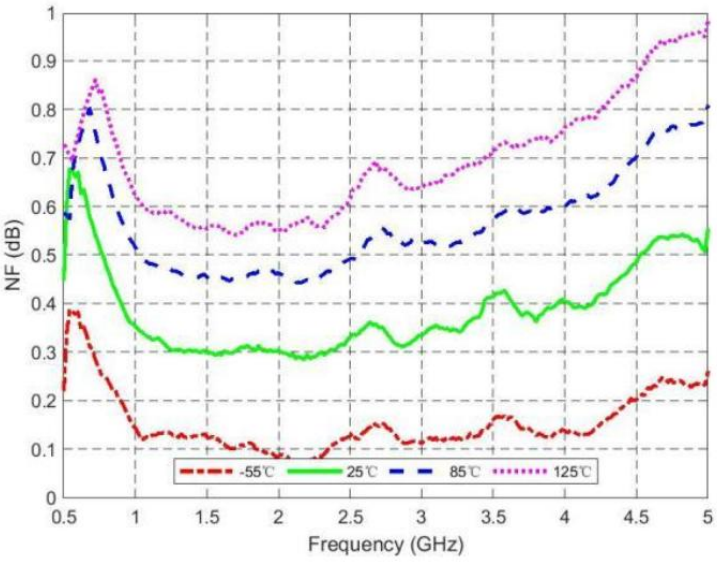
Output RL vs. Frequency vs. VD



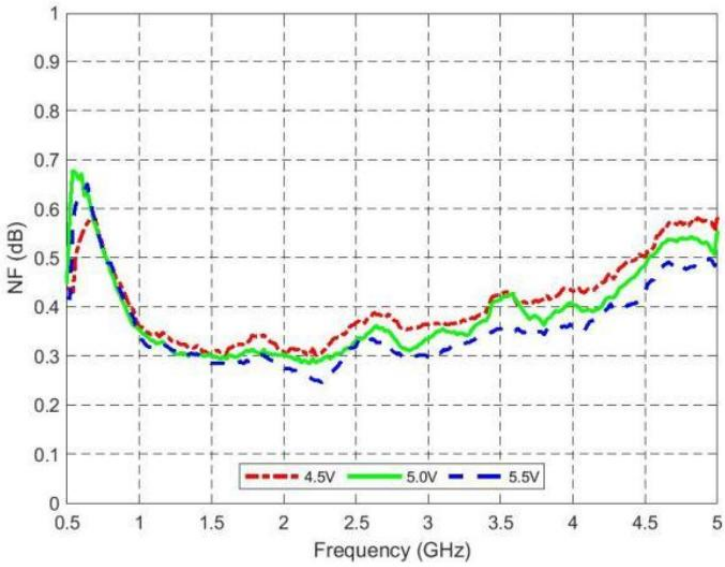
Isolation vs. Frequency vs. VD



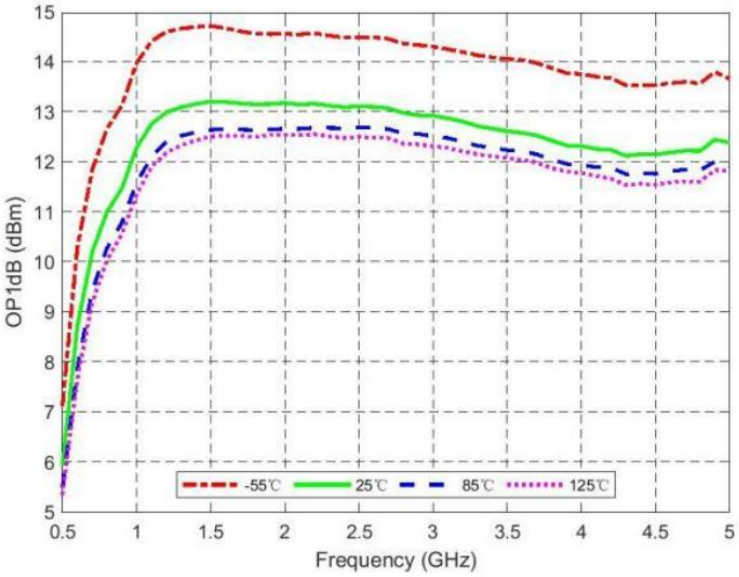
NF vs. Frequency vs. Temperature



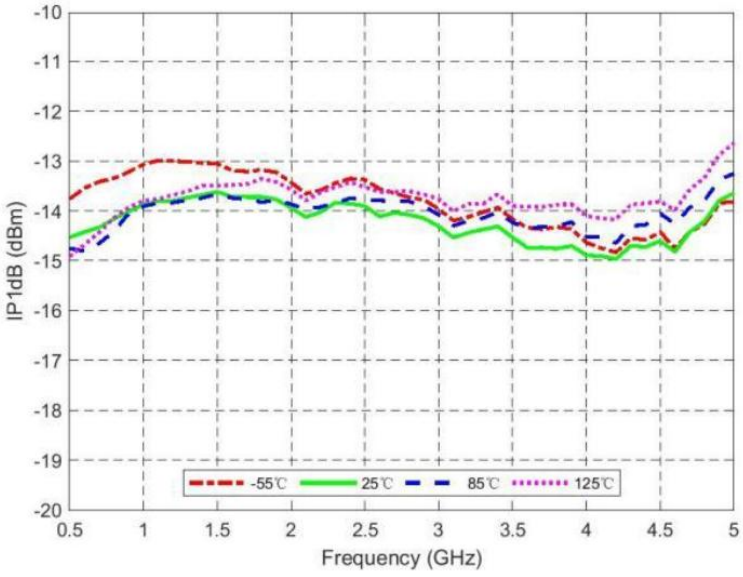
NF vs. Frequency vs. VD



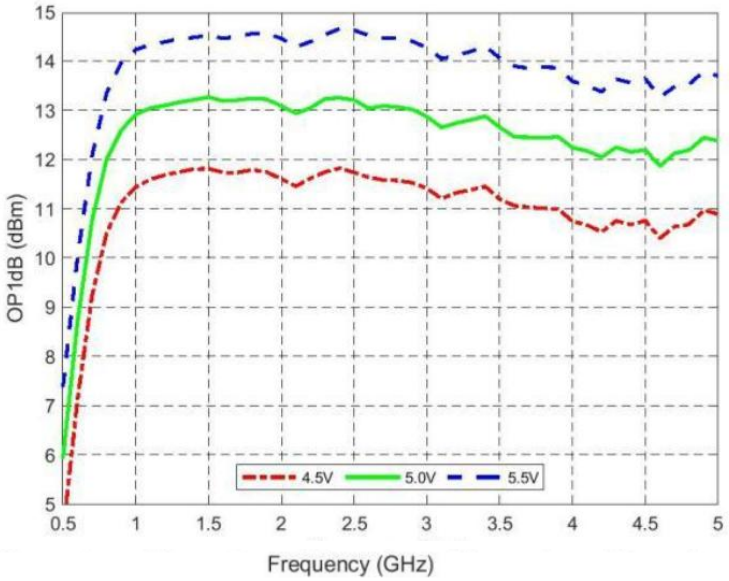
OP1dB vs. Frequency vs. Temperature



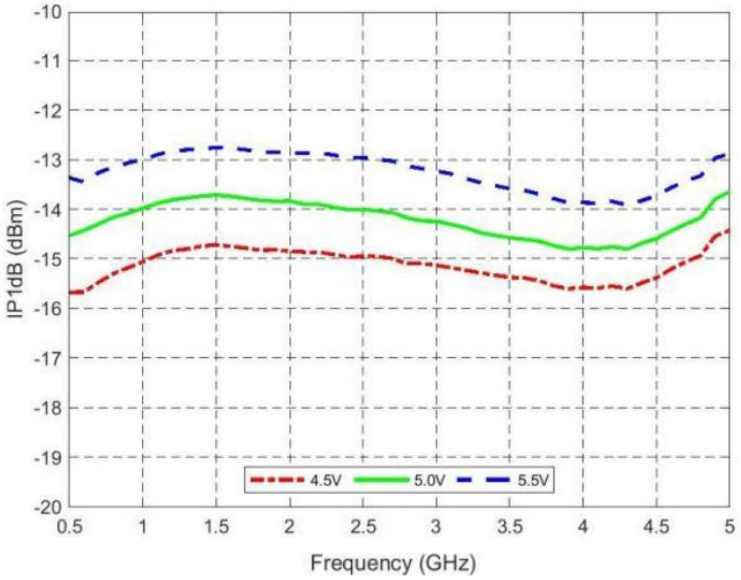
IP1dB vs. Frequency vs. Temperature



OP1dB vs. Frequency vs. VD

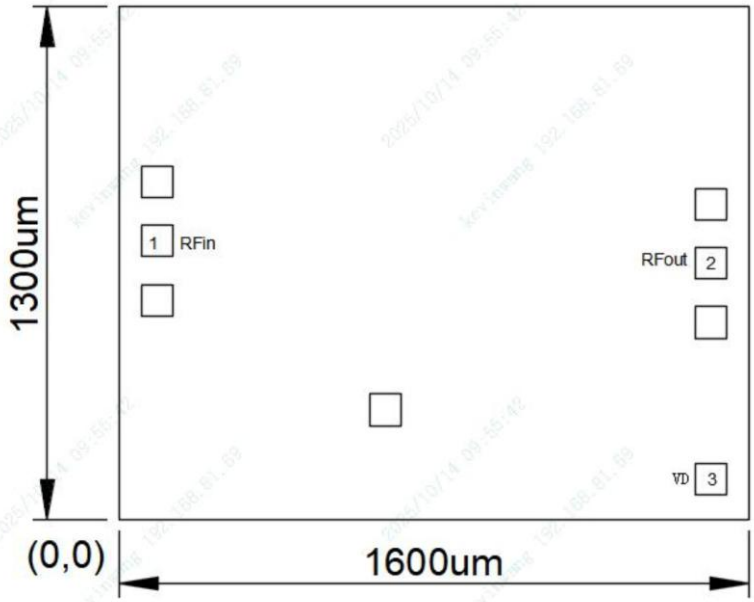


IP1dB vs. Frequency vs. VD



Outline Drawing:

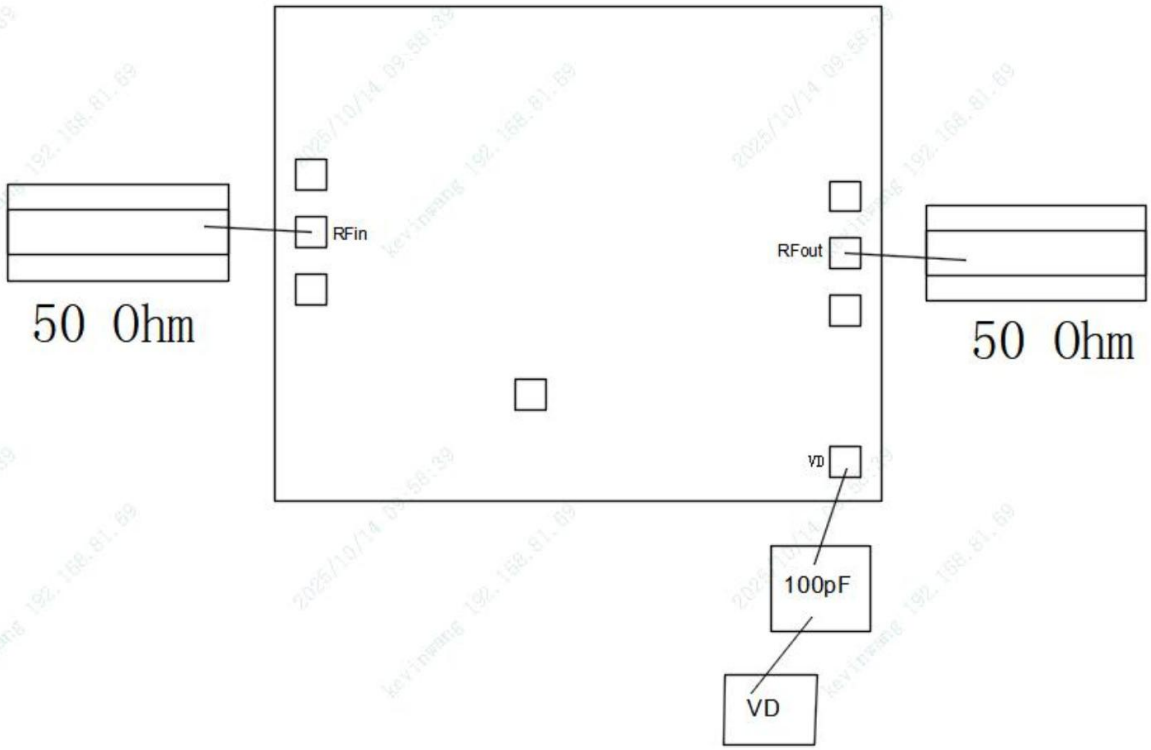
All Dimensions in um



Pad Description

Pad	Symbol	Pad Size (um)	Pad Coordinates (um)		Description
			X	Y	
1	RFin	80*80	97	706	RF input pad, 50Ω matched, external DC blocking capacitor not required.
2	RFout	80*80	1503	650	RF output pad, 50Ω matched, external DC blocking capacitor not required.
3	VD	80*80	1503	103.1	Drain Voltage

Assembly Drawing



Notes:

1. The bond wire length for the RF input is 950~1050μm, and for the RF output is 350~450μm.

2. Power-On Sequence

- Set ID limit to 100mA.
- Set VD = +5V. After powering on, IDQ is approximately 32.1mA.
- Apply RF signal.

3. Power-Off Sequence

- Turn off RF signal.
- Set VD to 0V.
- Turn off VD.

Notes:

4. Storage Conditions: The chip must be stored in an ESD-protective container in a nitrogen environment.

5. Cleaning Procedure: Bare dies must be handled and used in a clean environment. The use of liquid cleaning agents to clean the chip is strictly prohibited.

6. ESD Protection: Strictly adhere to ESD protection requirements to prevent electrostatic damage to the device.

7. General Handling: Use a vacuum tip or precision pointed tweezers to pick up the chip. Avoid touching the chip surface with tools or fingers during operation.

8. Assembly: Chips can be mounted using conductive epoxy adhesive. The mounting surface must be clean and flat. Epoxy Bonding Process: Control the dispensing volume of conductive epoxy based on the chip area. Apply an amount such that when the chip is placed in position, a small fillet of epoxy is visible around the periphery of the chip. Refer to the conductive epoxy manufacturer's datasheet for curing conditions.

9. Wire Bonding: Either ball bonding or wedge bonding is recommended using Φ 25um gold wire. The stage temperature is typically around 150°C. For ball bonding, the bonding force is typically 40~50 gf; for wedge bonding, the bonding force is typically 18~22 gf.

Maximum Ratings:

1. Power supply voltage VD: +6V
2. RF input power: +18dBm
3. Storage temperature: -65℃ to +150℃
4. Operating temperature: -55℃ to +125℃